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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,928	12/10/2003	Masakazu Fukuda	Q78869	6312

23373 7590 10/30/2006

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EXAMINER	
LAUTURE, JOSEPH J	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,928	FUKUDA, MASAKAZU	
	Examiner	Art Unit	
	Joseph Lauture	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

Applicant's amendment filed on 08/14/2006 has been entered. As a result, all 35 U.S.C 112 rejections have been overcome.

Response To Arguments

In a response posted 08/14/2006, applicant argued that Cabler (US 5,625,357) fails to teach two constant current sources. Figure (1) shows an FIR (50) which comprises two sources I_0 and I_1. Applicant further argues (See page 4) that only figure (1) teaches two current sources. Applicant is reminded that the examiner is free to consider any drawing of the patent which he/she deems to be relevant.

The applicant also argues (See page 5 of the remarks) that the circuit of Cabler requires more than two current sources and more than two dedicated pairs of inverted and non-inverted switches. However, Cabler does teach in figure (1) two current sources and the applicant claims two current sources.

The applicant further argues (See page 5 of remarks) that the Ledzius reference US 5,323,157) does not remedy the deficiency of Cabler (US 5,625,357). The examiner disagrees because Ledzius does teach in figure (3) a sigma delta DAC including a plurality of flip-flops (81-83) used as delay elements, each flip-flop having two outputs, each output coupled to a respective one of the MOS transistors (See figure (4); and column 6, lines 16-40). Cabler does not teach these limitations.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cabler (US 5,625,357) in view of Ledzius et al (US 5,323,157).

Regarding claim1, Cabler teaches in figure (1) a reconstruction filter apparatus, the apparatus comprising: a constant current source I_{REF} common to a plurality of resistive paths; a plurality of switches (B_0, B_1) arranged in cascade, each being operative to output data by controlling currents from the constant current source on the basis of each of the output data to thereby generate a plurality of weighted currents (See column 2, lines 34-39) that are weighted according to filter characteristics, the weighted currents being added separately for inverted and non-inverted (See switch connections to B_0 and B_1 in figure 2) and output at an output side of the FIR filter. Cabler also teaches that the use of two or more constant current sources to generate the plurality of weighted currents is a scheme well known in the art (Refer to current sources (52), (53) of figure (1)).

Cabler does not specifically teach a plurality of delay elements connected to MOS transistors as part of a delta-sigma modulator or of a digital signal processor. However, Ledzius et al teach in figure (3) a sigma-delta DAC including a plurality of flip-flops (81-83) used as delay elements, each flip-flop having two outputs, each output

coupled to a respective one (See fig (4) and column 6, lines 16-40) of the MOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Ledzius et al into the system of Cabler to improve system performance and reliability because that would provide improved signal-to-noise ratio and less complexity (See column 2, lines 3-5).

Regarding claims 2 and 3, Cabler teaches in figure (2) a current-to-voltage conversion unit shown in figure (4), said unit having an input side coupled to the output side (I_{OUT}) of the FIR filter and comprising a full differential operational amplifier (25) and a feedback resistors (30), said amplifier having a pair of inputs (See figure 4), each input coupled to a respective one of each separate output (I_{OUT}) of said FIR filter; a single differential conversion operational amplifier (27) on the output side of the full differential operational amplifier (25), the amplifier (27) having a pair of inputs, each input coupled to a respective one of each separate output of the FIR filter, and having an output side (37);

Regarding claims 4, 5 and 6, Cabler teaches in figure (2) a reconstruction filter apparatus, the apparatus comprising: a constant current source I_{REF} common to a plurality of resistive paths; a plurality of switches (B_0, B_1) arranged in cascade, each being operative to output data by controlling currents from the constant current source on the basis of each of the output data to thereby generate a plurality of weighted currents (See column 2, lines 34-39) that are weighted according to filter characteristics, the weighted currents being added and output at an output side of the FIR filter;

Cabler does not specifically teach a plurality of flip-flops connected to MOS transistors forming delay elements as part of a delta-sigma modulator or of a digital signal processor. However, Ledzius et al teach in figure (3) a sigma-delta DAC including a plurality of flip-flops (81-83) used as delay elements, each flip-flop having two outputs, each output coupled to a respective one (See fig (4) and column 6, lines 16-40) of the MOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Ledzius et al into the system of Cabler to improve system performance and reliability because that would provide improved signal-to-noise ratio and reduced complexity (See column 2, lines 3-5). It would have been further obvious to include such a filter apparatus in a digital signal processor, a delta-sigma modulator or any other data converter where a filter is needed.

Regarding claim 7, Cabler teaches a delta-sigma modulator wherein a constant current source comprises a common source for generating a plurality of weighted currents (See column 8, lines 20-23).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Lauture, whose telephone number is (571) 272-1805. The examiner can normally be reached Monday to Friday between 9:30 am and 6:00 PM

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached at (571) 272-7492. The fax number for the organization to which this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov.*** Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Rexford Barnie
REXFORD BARNIE
SUPERVISORY PATENT EXAMINER
10/26/06

Joseph Lauture
Art Unit: 2819
Date: 1016/2006